

## **CACHE MEMORY ARCHITECTURE AND ASSOCIATED MICROPROCESSOR DESIGN**

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### Abstract of the Disclosure

10 A single memory element, which may consist of general purpose SRAM chips,  
is used to implement both tag and data cache memory functions, resulting in an  
efficient, low cost implementation of high speed external cache memory. In one  
embodiment, a bank of general purpose random access memory used by a  
microprocessor as an external cache memory stores both cache tags and cache data in  
separate memory locations. During a read operation, the microprocessor retrieves a  
cache tag from the bank of general purpose random access memory before retrieving  
corresponding cache data therefrom, and compares the cache tag to a memory address to  
assess whether requested data resides within the cache memory. The microprocessor  
15 preferably accesses the bank of general purpose random access memory using a memory  
mapping function which maps the memory address into a cache tag address and a cache  
data address.

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